Abstract

LEO communication satellite systems typically utilize Active Phased Array antenna's because they are reliable and offer multiple beam operation, as well as electronic beam steering. The key technology behind the succesful realization of these systems is the GaAs MMIC-based module which is used to produce the active elements of the antenna.

The MMIC modules need to be capable of a variety of complex functions, while they simultaneously have to be reproducibly matched in their performance parameters to provide the desired beam shaping. This poses a challenge to the module manufacturer who has to produce hundreds or thousands of MMIC modules, all closely matched in their performance characteristics at affordable cost.

As the operating frequencies shift from the current L- and S-band systems to Ku- and Ka-band the challenge is even greater and novel technologies will have to be implemented to meet the new demands.

Introduction

Many applications exist or are planned which will use active phased array antennas for space communications systems. First generation systems such as Iridium and Globalstar are currently nearing completion and will soon be operational. These systems provide voice, data and paging services through the use of GaAs MMIC-based solid state phased arrays on satellites positioned in low earth orbits (LEO) and operate at L- and S-band frequencies. Next generation systems such as Teledesic and Skybridge will in all probability benefit even more from advanced solid state technology. These systems will have much more signal bandwidth at higher operating frequencies (Ku-, K-, Ka-band) in order to provide video, data and internet services to meet a growing global demand for network access.

Microwave Module Requirements

The enabling technology for all of these present and future systems is based on state-of-the-art solid state microwave devices, which are designed into active Transmit and Receive (T/R) modules. The key to the module technology is the Gallium Arsenide (GaAs) Monolithic Microwave Integrated Circuit (MMIC). This circuit technology allows the integration of advanced solid state devices such as Pseudomorphic High Electron Mobility Transistors (pHEMTs), along with the necessary passive circuit elements to make completely functional microwave circuits with the necessary performance requirements to realize the system. These performance requirements are summarized below:

- Multitone signal amplification at best possible efficiency
  - The gain per module can run as high as 60 dB
  - Output power levels ranging from 2-15 watts
- Phase control and trimming capability
  - Modules need to be phase matched to within a few degrees or less
  - Modules need to phase track over temperature variations and varying output power levels while maintaining the match
- Amplitude matching
  - Modules need to be matched for amplitude to within a few tenths of a dB over temperature and output power variations
- Output power adjustability
  - Variability of output power level by supply voltage control from 100% down to 10%, while maintaining efficiency and linearity
- Linearity
  - Amplifiers typically need to operate at 15-16 dB Noise Power Ratio (NPR) over varying power levels
- Overdrive protection
  - In multitone operating systems large amplitude spikes can travel through the RF amplification chain, driving varying stages deep into compression (more than 6 dB).

By choosing the appropriate device technology combined with circuit design and manufacturing methods highly integrated modules can be mass produced that meet both the performance demands and the cost objectives. Typically the device technology of choice is the pHEMT which provides the necessary attributes to meet the previously outlined performance requirements.

Circuit functions such as multistage amplifiers, phase shifter bits, attenuators and switch functions can be all integrated on GaAs chips. Since these MMIC chips are processed on semiconductor wafers using batch processing and photolithographic techniques, they can be very repeatable from one chip to the next. The use of interconnected groups of these chips in T/R modules makes an inherently reproducible product, as chip interfaces are minimized and kept to a 50 ohm level, minimizing the types of VSWR interactions that are typically seen between microwave components.

The demands of phase and amplitude matching can be met by taking advantage of MMIC reproducibility combined with automated pick and place and wire bonding techniques. This approach was used in the fabrication of the Iridium™ and Globalstar modules. A typical S-band transmit module is shown in Figure 1. This module uses GaAs MMIC chips to provide power amplification. The basic transmit module is a hermetically sealed unit that also contains various support circuits that maintain fail safe operation of the microwave circuits during routine antenna operation.

Figure 2 shows a composite plot of the output power versus Noise Power Ratio (NPR) of 120 S-band transmit modules at four different operating voltages showing tracking over power level (noise loaded operation). It is also showing the variations introduced by the various manufacturing operations such as wafer fabrication, die attachment and placement, wire bonding and testing variability.

Next Generation Technology

Future solid Ka-band communications systems will require electrical performance surpassing that achieved by the modules shown. Future system performance requirements call for nearly 3 dB improvement in the overall system sensitivity and the improvement budget has been apportioned among various software and hardware designs. A new version of the T/R module is expected to achieve improved system sensitivity through a combination of increased power density and improved noise figure by using advanced pHEMT MMIC devices.

Through the use of pHEMT technology, an improvement in power added efficiency of nearly 2.0 dB and an improvement in the receive noise figure of almost 1.0 dB can be achieved at X-band over modules using MESFET MMICs. Furthermore, no increase in DC current consumption will be required to achieve this increased performance as the pHEMT devices are more efficient than their MESFET counterparts. The most cost effective development path to future systems operating at Ku-band and above will leverage from prior experience. At 19 GHz and above, conventional chip and wire module designs may not be adequate, and novel integration techniques need to be employed to meet the previously described performance requirements.

Flat Panel Phased Array Technology

Conventional modules utilizing automatic assembly and test methodology sell for anywhere between $3,000 and $5,000 depending on the complexity. To enable affordable solid state phased arrays for commercial applications, arrays must be built with element costs of less than $50, including MMIC circuitry. In 1995 Raytheon initiated a program to develop a low cost, flat panel phased array designed to reduce equivalent module costs to below $50 each. This program is jointly sponsored by DARPA and Raytheon.

The concept is very simple. It involves much higher levels of integration than have previously been done in GaAs, effectively reducing the microwave circuitry to one or two highly integrated chips. All microwave, digital control, switching and several other functions are integrated onto this chip or chips. These chips are then attached directly to the backplane of a phased array antenna. The basic concept is shown in Figure 3, a sketch depicting a flat panel array having patch radiating elements, transmit or receiver channels consisting of one or two GaAs MMIC chips and bypass capacitors and a mutlilayer board having the rf binary feed network. In this concept a high level of integration in the array is achieved by multiplexing digital control signals and dc bias voltages on the rf corporate feed network for the array. Using this concept it is felt that a thin, flat panel array antenna can be built for use at Ku or Ka-band, in which the transmit or receive module elements would cost between $35 and $50 per element
During the past two years Raytheon has been working to demonstrate the flat panel array technology for use in a 20 GHz receive array. The Raytheon Advanced Device Center has been actively working in two general areas, chip set design for the unit cell and advanced development of interconnect and bonding techniques to support flat panel assembly. Work in the chip area has progressed to the point where initial iterations of an advanced pHEMT low noise amplifier and a D/MMIC multi-function chip are complete and being evaluated. In parallel, technology work is proceeding on

advanced concepts for die attach and interconnecting chips to array I/Os without the use of wirebonds. The following paragraphs describe some of the details of these efforts.

Unit Cell Design

The design of a cost effective unit cell is key to achieving the goal of a low cost, thin, flat panel phased array communications antenna. Of necessity, all of the functionality of a receive or transmit array element must fit in a planar format behind the basic element lattice of the array. With the triangular grid required by the scan characteristics of a receive array at 20 GHz, the maximum planar dimension of the flat panel demonstration array is 290 mils. All electronic, interconnection and any incidental bias or bypass circuitry must fit within this area in order to allow the use of a low cost planar hybrid circuit format. Of course, the unit cell must also meet its electrical requirements in order to build a functional array.

In the case of the flat panel array program, it has been determined that switchable polarization is required. This places a requirement on the receive element that it be capable of either right hand or left hand circular polarization. This requirement complicates the LNA and the digital circuitry that drives it, but also makes the flat panel design attractive to multiple user communities. A block diagram of the unit cell is shown in Figure 4. It shows polarization switch on the upper left, feeding the low noise amplifier MMIC. The rf path is completed through the phase shifter, attenuator and diplexer as shown. The diplexer consists of a high pass and low pass filter which is transparent to the rf going through it from the phase shifter/attenuator, but which strips off the baseband signal with the digital control information. The baseband signal goes to a decoder/control logic block which detects it and converts the modulated signal to a serial data stream. The serial data stream is used to feel the shift register, which converts it to a parallel word and compares it to an address which is hard wired into the unit cell at the time of manufacture. If the instruction is for the particular unit cell, the appropriate states are latched and fed to the LNA control lines, the phase shifter and the attenuator. Drain switching is used in the LNA to turn it on and off, while signals are provided to switch to either right or left hand circular polarization. The phase shifter and attenuator use complimentary drive signals to switch in the proper state. Not shown on the block diagram, but still essential to the operation of the unit cell are the bias inputs with their attendant bypassing and decoupling elements.

The working requirements for the unit cell are as follows:

Frequency Range	19.2 - 21.2 GHz
Gain	16 dB
Noise Figure	3.5 dB
Polarization	Switchable RHC-LHC
Size	Fit within .290"X.245" Area
Digital Control	Baseband Serial Data Stream

The LNA chip is designed to have 27 dB of gain and 2.5 dB noise figure in order to offset the 10 dB loss of the phase shifter and 1.0 dB projected loss of the polarization switch.

Figure 5 is a layout of the unit cell. The unit cell contains five coaxial inputs which serve as the interface points to the array multi-level board. They will initially be designed to be co-planar with the surface on which the chips are mounted. The first generation design will use one mil wire bonds for the interface with the rest of the array circuitry. An alternative to wire bonds in the future could be the Raytheon DBIT or Direct Backside Interconnect Technology system. This concept will offer the prospect of connecting chip I/Os to the coax feed-throughs without wire bonds, greatly reducing the impact of parasitic inductance in the interface and minimize path length differences which give rise to phase variations between elements or cells, thus solving the phase and amplitude matching requirements. Present DBIT demonstrations have shown low loss and low VSWR up to 25 GHz with future versions showing good performance to 40 GHz. Considerable work, however, needs to be done to make this a viable technology. The following is an example of an element design.

Switch/Low Noise Amplifier Design

A design of an LNA switch MMIC assembly was carried out centered around the use of a 0.25μ pHEMT LNA process (MMC-55). This process produces attractive low noise characteristics through the use of T-gates on an MBE-grown epitaxial wafer. Figure 7 is the physical layout of a 20 GHz LNA demonstration chip showing four FET amplifier stages. Initial results show that it achieves about 27 dB of gain with about 2.7 dB noise figure including the switch loss.

Multifunction MMIC Chip Design

The multifunction chip provides all of the digital decoding and control and the microwave phase shift and attenuation functions for the flat panel array unit cell. The microwave portions of the chip operate over a frequency band of 19.2 to 21.2 GHz, as does the switch/LNA chip. The chip must provide four bits of phase shift (for beam steering) and one bit of attenuation (for array calibration). Specifications on return and insertion losses have been determined on the basis of interfacing the chip into the array with the switch/LNA chip. The digital portion of the chip must separate the rf received signals from the baseband control signals and then convert the baseband signal into a serial data stream which controls the phase shifter, attenuator and front-end switch devices. The baseband signal is detected and then goes into a Schmitt trigger circuit which then feeds the serial to parallel shift register, latches and level shifters. Comparators are used to compare the address portion of the serial data stream to a word which is coded into the unit cell with wire bonds at the time of manufacture. The block diagram of the multifunction chip is shown in Figure 7. The entire chip is realized in GaAs MMIC form which has the added advantage in that it is radiation hard.

Advanced Interconnection Technology

Conventional modules use either single or multiple wirebonds to provide interconnects. One mil wire, however, represents about 0.0159 nHy per linear mil of inductance. For a typical wire bond length of 20 mils this means nearly .32 nHys of inductance, or nearly 40 ohms of inductive reactance at the input and output of the chip. It would be highly desirable to eliminate this inductance from the RF path if possible. In addition, wire bond length and loop variations are responsible for phase variations from module to module which are detrimental to operation of phased array antennas. Some companies are busy developing flip chip technology to reduce or eliminate the parasitic inductances caused by wire bonds. Flip chips represent blind connections to the mating circuitry and preclude optical inspection, which is used to detect many assembly faults in present hybrid operations. Flip chip MMIC chips typically need coplanar structures which tend to take up more chip area than microstrip design topologies.

An answer which Raytheon is implementing to determine its suitability for rf interconnects is our Direct Backside Interconnect Technology (DBIT). This concept uses via holes to carry circuit traces and grounds from the front side of the chip to the back side where they can then be bonded to the interfacing circuitry using either epoxy or solder techniques. Figure 9 shows a photograph of how a DBIT MMIC chip is interfaced to a patterned substrate. The photograph shows a 20 GHz LNA which was mounted to an alumina substrate using DBIT techniques. The rf input and output for the amplifier chip shown are connected to small pads on the backside of the chip. RF grounds are also brought through via holes in close proximity to the rf feedthroughs. A patterned die attach material is used to connect the chip to the interfacing circuitry. Gold bumps are used to raise the chip off the interconnecting substrate in order to keep it from shorting out when the chip is placed in the conductive epoxy bumps used to attach the chip to the substrate.

Figure 9 shows measured results for a group of 20 GHz LNAs mounted and tested on a DBIT alumina substrate. These results show that the input and output VSWRs and the gain of the amplifier is not subject to the kinds of VSWR interactions normally seen with wire bonds. Performance is excellent throughout the frequency range of interest and beyond. The present DBIT structure in the future could provide a truly low cost method for making high quality rf interconnects. In combination with the thermoplastic bonding materials described above, it offers the prospect of an assembly routine where an epoxy dispense machine is used to "write" the dots where the die will be attached and the rf interconnections will be made. This represents a low cost approach to achieving best possible rf performance. Wire bonds will, of course, still have to be used for dc interconnects and for personalization of the unit cell location in the array. These wires, however, do not handle rf and are therefore much less critical in determining rf performance than they formerly were.

Conclusions

The performance demands for solid state active array antennas for the newly planned satellite communications systems operating at K-and Ka -band can be met by the implementation of MMIC technology combined with novel design and assembly techniques such as flat panel technology and DBIT bond wire free die attachment techniques. These technologies are currently undergoing engineering evaluation and refinements and should be available for large scale manufacturing by the year 2000.

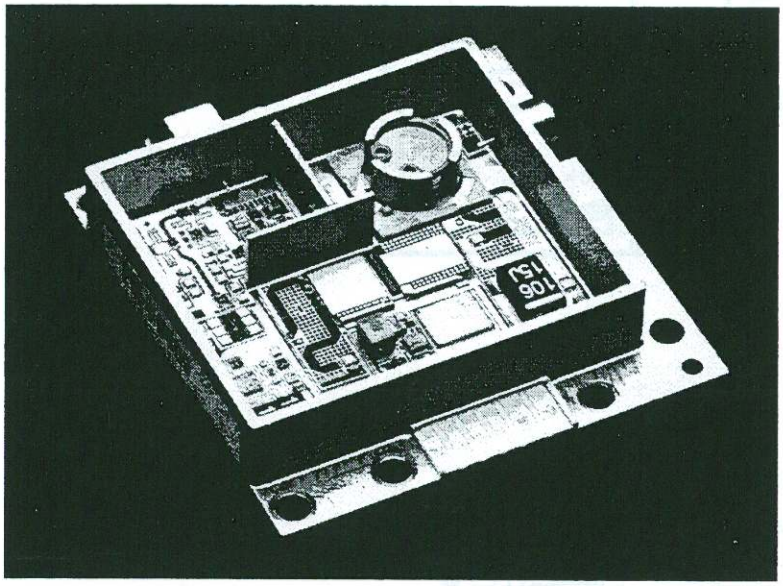

Figure 1. S-band Transmit module using GaAs MMICs

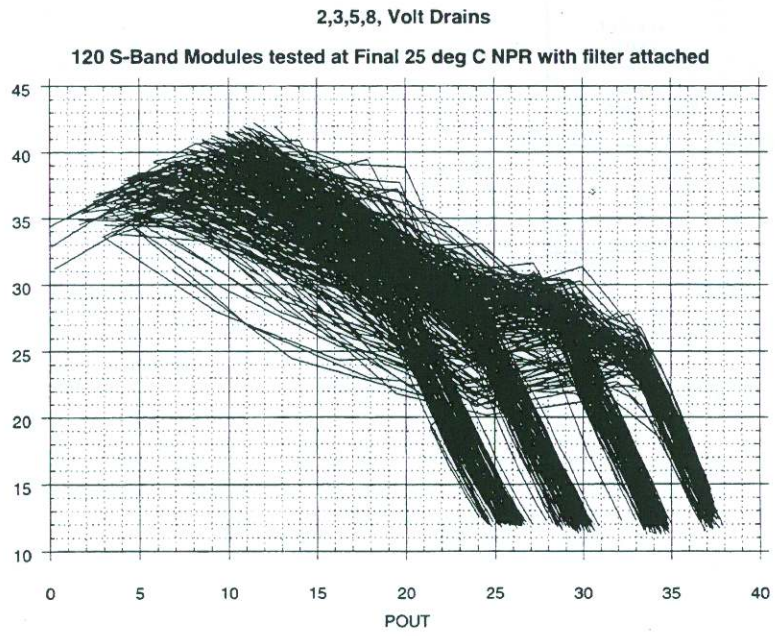

Figure 2. 120 S-Band Modules Tested at Final 25°C NPR with Filter Attached

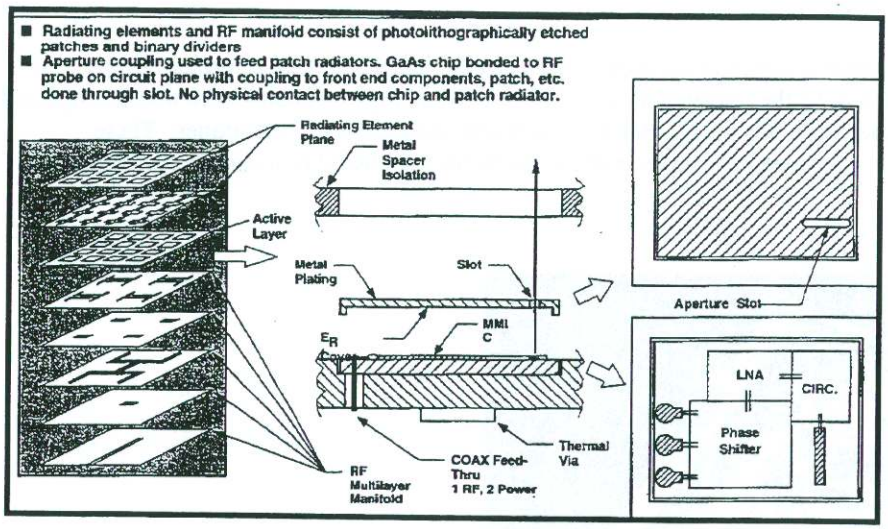

Figure 3. Low Cost Array Interconnect Approach

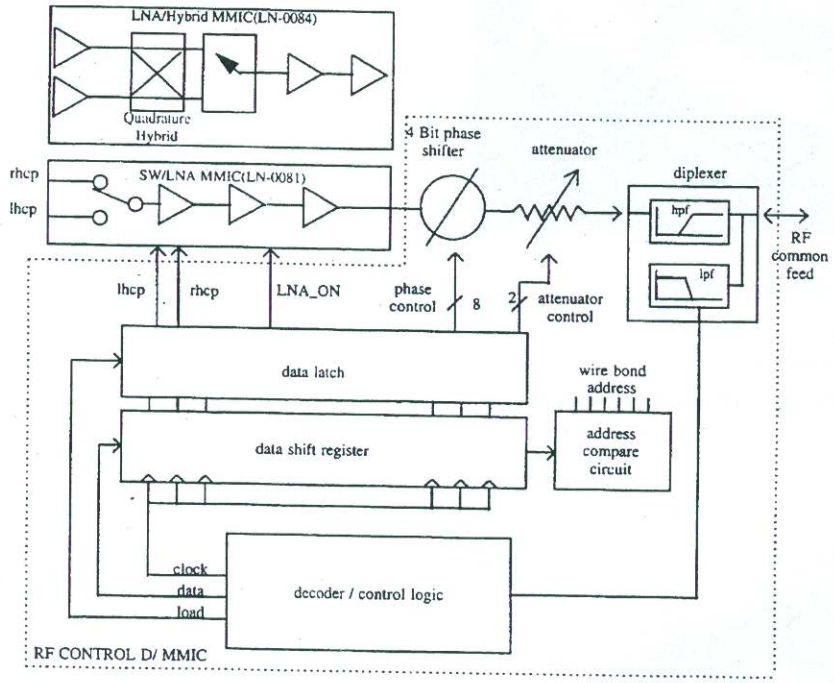

Figure 4. Block Diagram of Flat Panel Array Unit Cell.

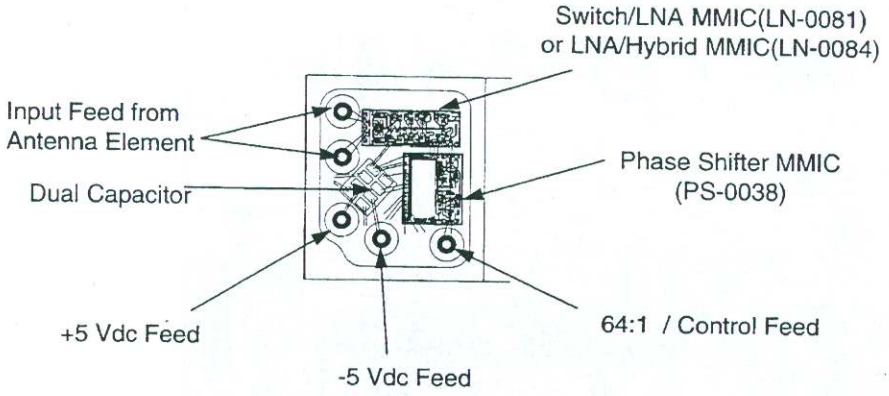

Figure 5. Layout of Flat Panel Array Unit Cell.

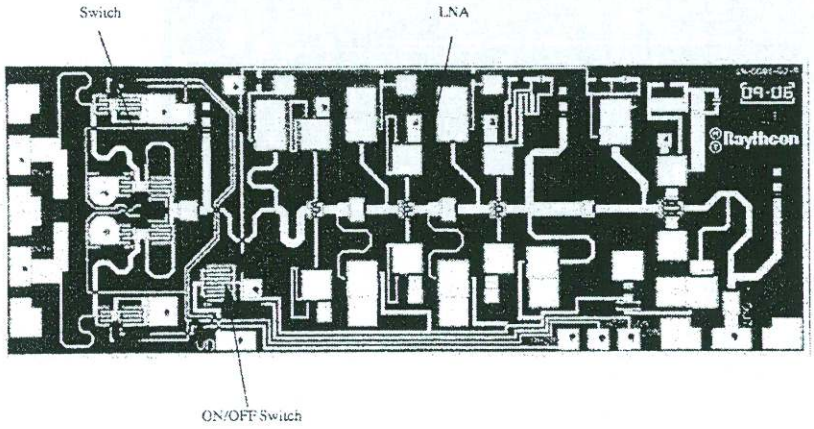

Figure 6. Layout (or photo) of LNA chip.

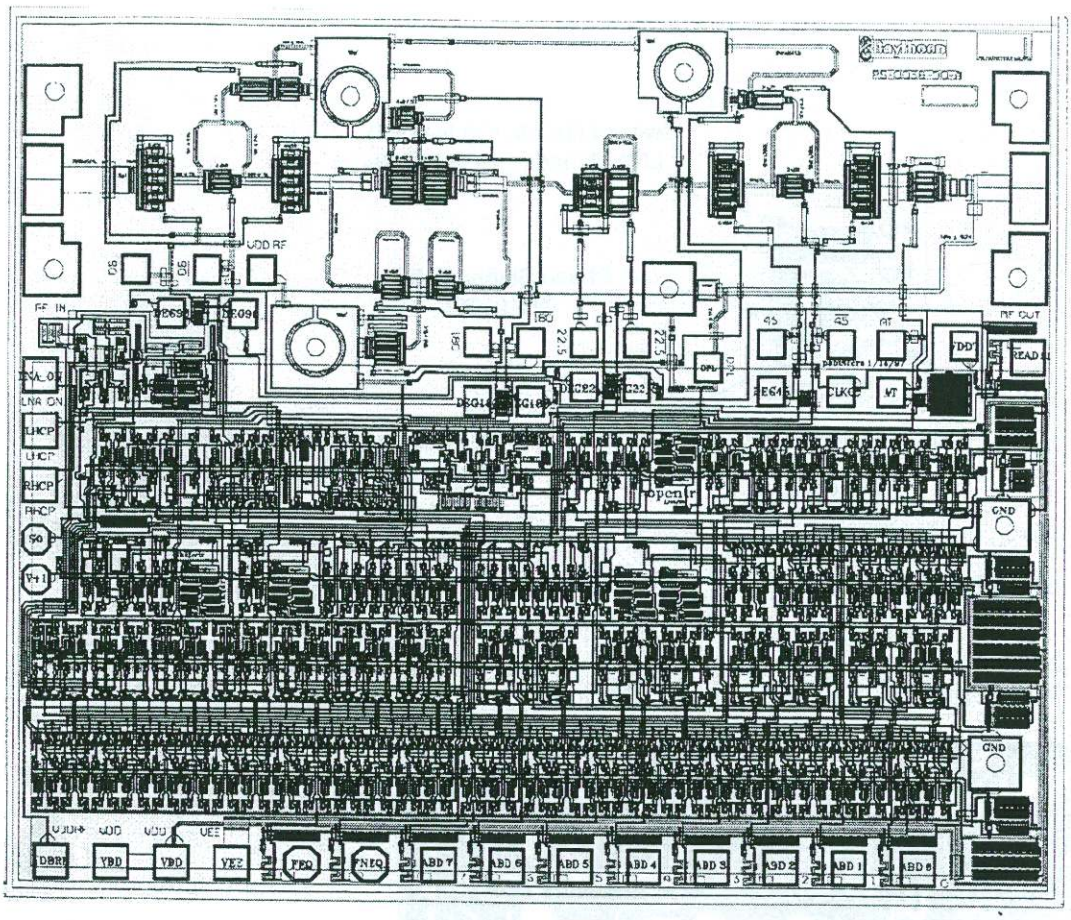

Figure 7. Multifunction Chip Block Diagram

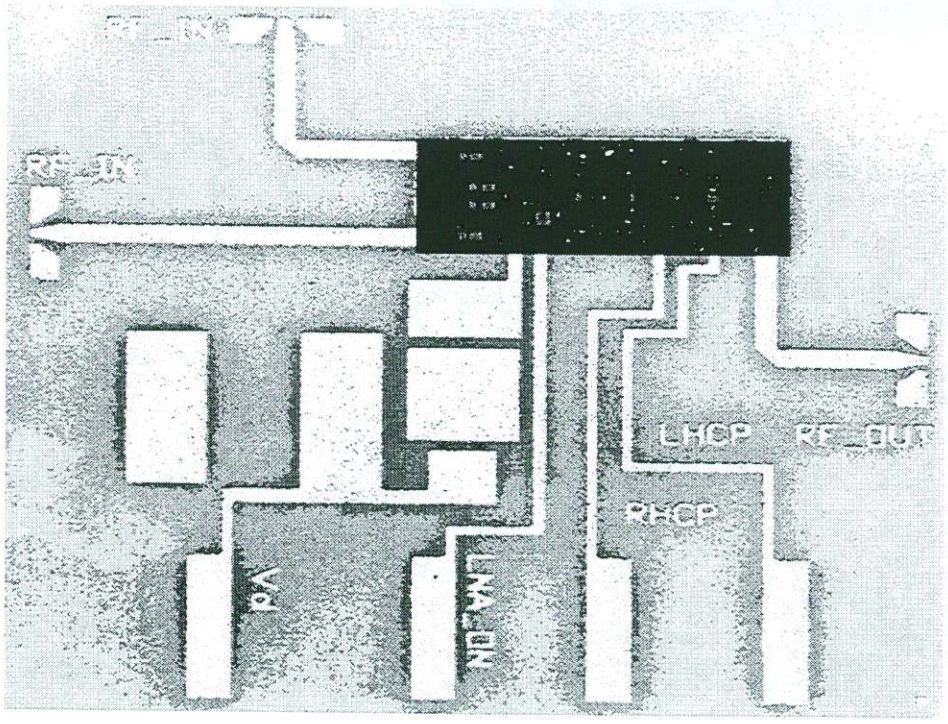

Figure 8. 20 GHz LNA chip mounted on DBIT substrate.

■ Switch/LNA Gain - 8 Carriers

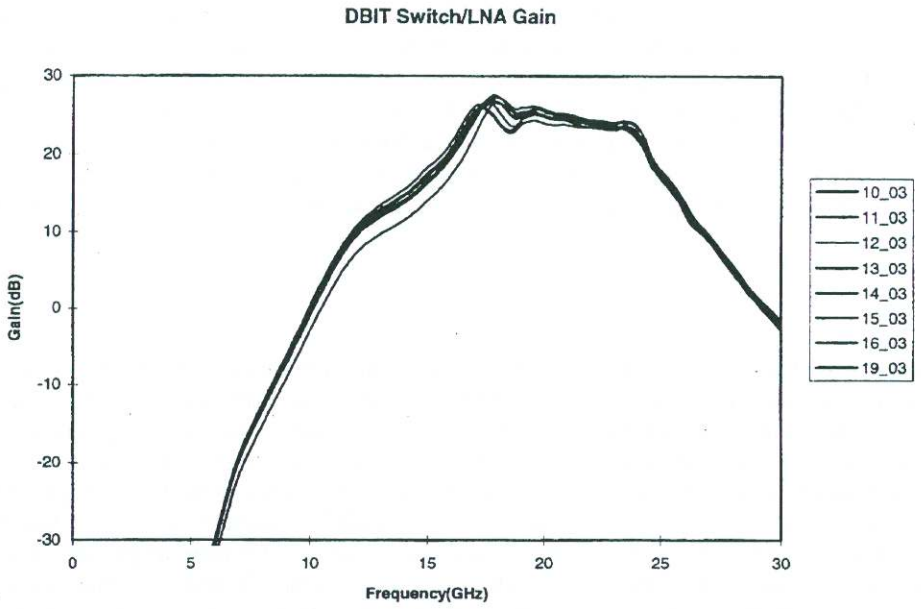

Figure 9. Measured results on 20 GHz LNAs measured in DBIT substrates.